STK5C4U332J-E

Advance Information

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Inverter IPM for 3-phase Motor Drive

Overview

This “Inverter IPM” is highly integrated device containing all High Voltage (HV) control from HV-DC to 3-phase outputs in a single DIP module (Dual-In line Package). Output stage uses RC-IGBT technology and implements Under Voltage Protection (UVP). Internal Boost diodes are provided for high side gate boost drive.

Function

- Single control power supply due to Internal bootstrap circuit for high side pre-driver circuit
- All control input and status output are at low voltage levels directly compatible with microcontrollers.
- Built-in cross conduction prevention.
- Externally accessible embedded thermistor for substrate temperature measurement

Certification

- UL1557 (File number: E339285).

Specifications

Absolute Maximum Ratings at Tc = 25°C

Parameter	Symbol	Remarks	Ratings	Unit
Supply voltage	V_{CC}	P to U-, V-, W-, surge < 500V *1	450	V
Collector-emitter voltage	V_{CE}	P to U, V, W or U, V, W, to U-, V-, W-	600	V
Output current	Io	P,U-,V-,W-,U,V,W terminal current	±3	A
		P,U-,V-,W-,U,V,W terminal current, Tc = 100°C	±1.5	A
Output peak current	Iop	P,U-,V-,W-,U,V,W terminal current, P.W. = 1ms	±6	A
Pre-driver voltage	VD1,2,3,4	VB1 to U, VB2 to V, VB3 to W, V_{DD} to V_{SS} *2	20	V
Input signal voltage	V_{IN}	HIN1, 2, 3, LIN1, 2, 3	−0.3 to V_{DD}	V
FLTEN terminal voltage	VFLTEN	FLTEN terminal	−0.3 to V_{DD}	V
RCIN terminal voltage	VRCIN	RCIN terminal	−0.3 to V_{DD}	V
ITRIP terminal voltage	VITRIP	ITRIP terminal	5	V
Maximum power dissipation	Pd	RC-IGBT per 1 channel	11.3	W
Junction temperature	Tj	RC-IGBT, Pre-Driver IC	150	°C
Storage temperature	Tstg		−40 to +125	°C
Operating case temperature	Tc	IPM case	−20 to +100	°C
Tightening torque		A screw part *3	0.6	Nm
Isolation Voltage	Vis	50Hz sine wave AC 1 minute *4	2000	VRMS

Reference voltage is “V_{SS}” terminal voltage unless otherwise specified.

*1: Surge voltage developed by the switching operation due to the wiring inductance between P and U-(V-, W-) terminal.

*2: Terminal voltage: VD1=VB1-U, VD2=VB2-V, VD3=VB3-W, VD4= V_{DD}-V_{SS}.

*3: Flatness of the heat-sink should be 0.15mm and below.

*4: Test conditions : AC2500V, 1 second.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

Electrical Characteristics at Tj = 25°C, VD1, VD2, VD3, VD4 = 15V

Parameter	Symbol	Conditions	Test circuit	MIN	TYP	MAX	Unit
Power output section							
Collector-emitter cut-off current	I_{CE}	V_{CE} = 600V	Fig.1	-	-	100	μA
Bootstrap diode reverse current	IR(BD)	VR(BD) = 600V	Fig.1	-	-	100	μA
Collector to emitter saturation voltage	V_{CE}(SAT)	Io = 3A, Tj = 25°C	Fig.2	-	1.6	2.4	V
		Io = 1.5A, Tj = 100°C			1.3	-	V
Diode forward voltage	VF	Io = 3A, Tj = 25°C	Fig.3	-	1.5	2.3	V
		Io = 1.5A, Tj = 100°C			1.3	-	V
Bootstrap ON Resistance	RB	IB = −1mA	Fig.4		110	300	Ω
Junction to case thermal resistance	θj-c(T)	RC-IGBT	-	-	-	11	°C /W
Control (Pre-driver) section							
Pre-driver power dissipation	ID	VD1,2,3 = 15V	Fig.5	-	0.1	0.2	mA
		VD4 = 15V		-	1.3	2.6	mA
High level Input voltage	Vin H	HIN1,HIN2,HIN3, LIN1,LIN2,LIN3 to V_{SS}	-	2.5	-	-	V
Low level Input voltage	Vin L	HIN1,HIN2,HIN3, LIN1,LIN2,LIN3 to V_{SS}	-	-	-	0.8	V
Logic 1 input leakage current	I_{IN+}	VIN = +3.3V	-	-	100	143	μA
Logic 0 input leakage current	I_{IN-}	VIN = 0V	-	-	-	2	μA
FLTEN terminal sink current	IoSD	FAULT:ON / VFLTEN = 0.1V	-	-	2	-	mA
FLTEN clearance delay time	FLTCLR	From time fault condition clear	-	1.0	2.0	3.0	ms
FLTEN Threshold	VEN+	VEN rising	-	-	-	2.5	V
	VEN-	VEN falling	-	0.8	-	-	V
ITRIP threshold voltage	VITRIP	ITRIP(10) to V_{SS}(1)	-	0.44	0.49	0.54	V
ITRIP to shutdown propagation delay	t_{ITRIP}		-	-	550	-	ns
ITRIP blanking time	$t_{ITRIPBL}$		-	100	350	-	ns
V_{CC} and V_{BS} supply undervoltage protection reset	V_{CCUV+} V_{BSUV+}		-	10.5	11.1	11.7	V
V_{CC} and V_{BS} supply undervoltage protection set	V_{CCUV-} V_{BSUV-}		-	10.3	10.9	11.5	V
V_{CC} and V_{BS} supply undervoltage hysteresis	V_{CCUVH} V_{BSUVH}		-	0.14	0.2	-	V

Reference voltage is “V_{SS}” terminal voltage unless otherwise specified.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Electrical Characteristics at Tj = 25°C, VD1, VD2, VD3, VD4 = 15V, V_{CC}=300V, L=3.9mH

Parameter	Symbol	Conditions	Test circuit	MIN	TYP	MAX	Unit
Switching Character							
Switching time	t ON	Io = 3A	Fig.6	-	0.5	1.2	μs
	t OFF			-	0.6	1.4	
Turn-on switching loss	Eon	Io = 1.5A	Fig.6	-	100	-	μJ
Turn-off switching loss	Eoff			-	15	-	μJ
Total switching loss	Etot			-	115	-	μJ
Turn-on switching loss	Eon	Io = 1.5A, Tj = 100°C	Fig.6	-	120	-	μJ
Turn-off switching loss	Eoff			-	20	-	μJ
Total switching loss	Etot			-	140	-	μJ
Diode reverse recovery energy	Erec	I_F = 1.5A, V_{CC} = 300V, Tc = 100°C	-	-	35	-	μJ
Diode reverse recovery time	trr		-	-	150	-	ns
Reverse bias safe operating area	RBSOA	Io = 6A, V_{CE} = 450V	-	Full square			-
Short circuit safe operating area	SCSOA	V_{CE} = 400V, Tj = 100°C	-	3	-	-	μs

Reference voltage is "V_{SS}" terminal voltage unless otherwise specified.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Notes

1. When the internal protection circuit operates, a Fault signal is turned ON (When the Fault terminal is low level, Fault signal is ON state : output form is open DRAIN) but the Fault signal does not latch.After protection operation ends,it returns automatically within about typ. 2ms and resumes operation beginning condition. So, after Fault signal detection, set all input signals to OFF (Low) at once. However, the operation of pre-drive power supply low voltage protection (UVLO:with hysteresis about 0.2V) is as follows.

   Upper side:
   The gate is turned off and will return to regular operation when recovering to the normal voltage, but the latch will continue till the input signal will turn 'low'.
   Lower side:
   The gate is turned off and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.

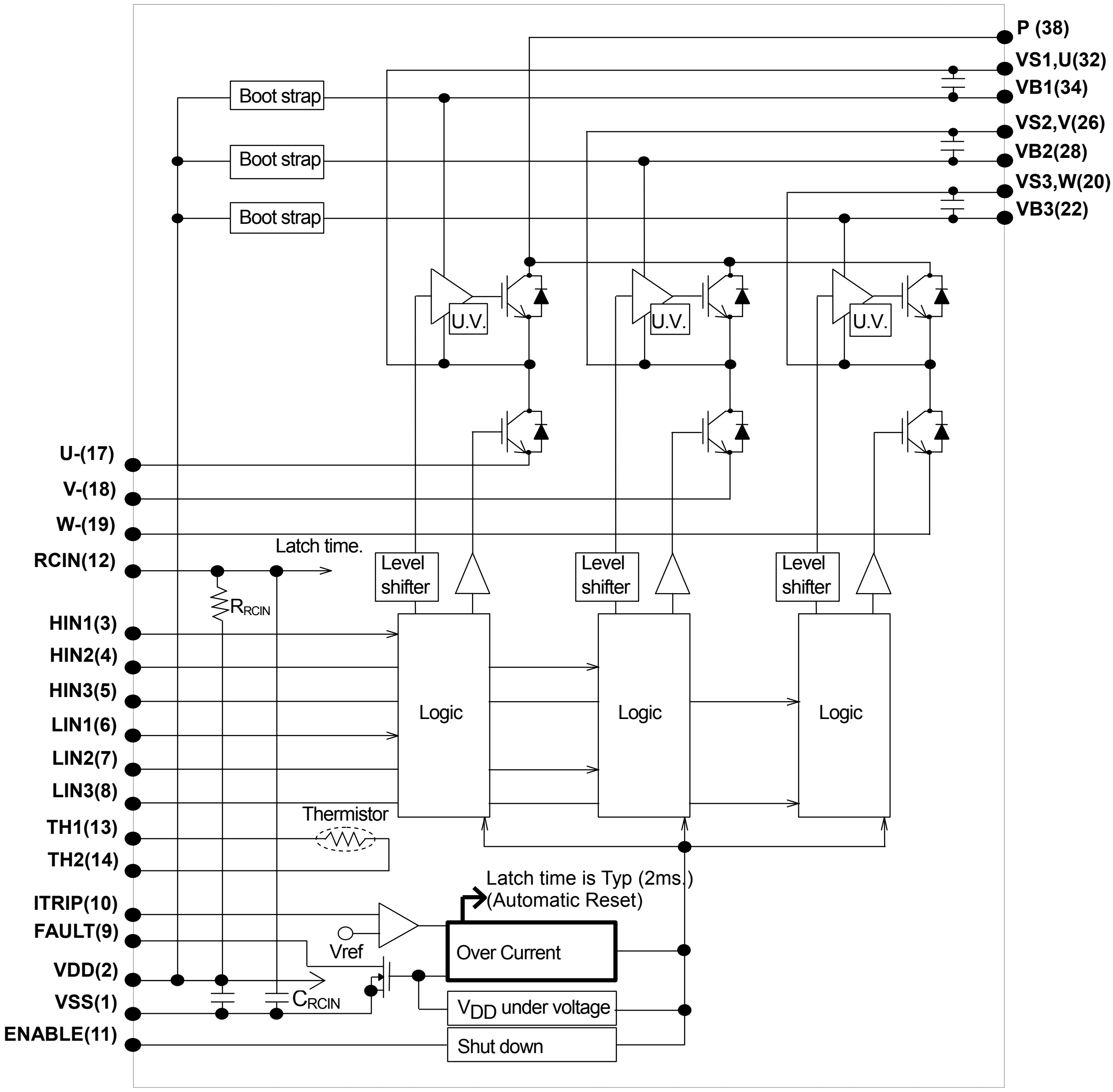
2. When assembling the IPM on the heat sink with M3 type screw, tightening torque range is 0.4 Nm to 0.6 Nm.

3. When use the over-current protection with external resistor, please set resistance value so that current protection value becomes equal to or less than the double (2 times) of the rating output electric current (Io).

Module Pin-Out Description

Pin	Name	Description
1	VSS	Negative Main Supply
2	VDD	+15V Main Supply
3	HIN1	Logic Input High Side Gate Driver - Phase U
4	HIN2	Logic Input High Side Gate Driver - Phase V
5	HIN3	Logic Input High Side Gate Driver - Phase W
6	LIN1	Logic Input Low Side Gate Driver - Phase U
7	LIN2	Logic Input Low Side Gate Driver - Phase V
8	LIN3	Logic Input Low Side Gate Driver - Phase W
9	FAULT	Fault output
10	ITRIP	Current protection pin
11	ENABLE	Enable input
12	RCIN	FAULTCLR time setting terminal
13	TH1	Thermistor output
14	TH2	Thermistor output
15	-	Without pin
16	-	Without pin
17	U-	Low Side Emitter Connection - Phase U
18	V-	Low Side Emitter Connection - Phase V
19	W-	Low Side Emitter Connection - Phase W
20	W, VS3	Output 3 - High Side Floating Supply Offset Voltage
21	-	Without pin
22	VB3	High Side Floating Supply Voltage 3
23	-	Without pin
24	-	Without pin
25	-	Without pin
26	V,VS2	Output 2 - High Side Floating Supply Offset Voltage
27	-	Without pin
28	VB2	High Side Floating Supply voltage 2
29	-	Without pin
30	-	Without pin
31	-	Without pin
32	U,VS1	Output 1 - High Side Floating Supply Offset Voltage
33	-	Without pin
34	VB1	High Side Floating Supply voltage 1
35	-	Without pin
36	-	Without pin
37	-	Without pin
38	P	Positive Bus Input Voltage

Equivalent Block Diagram



Test Circuit

(The tested phase : U+ shows the upper side of the U phase and U- shows the lower side of the U phase.)

■ ICE / IR(BD)

	U+	V+	W+	U-	V-	W-
M	38	38	38	32	26	20
N	32	26	20	17	18	19

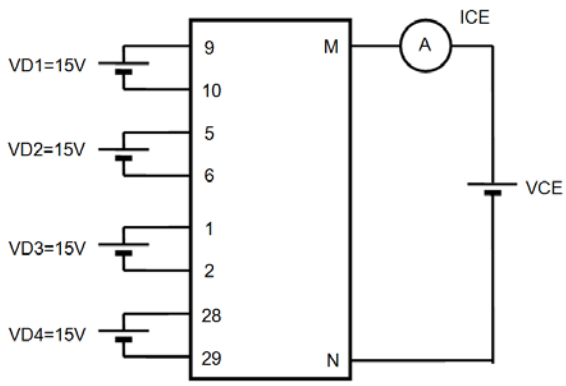


Fig.1

■ VCE(SAT) (Test by pulse)

	U+	V+	W+	U-	V-	W-
M	38	38	38	32	26	20
N	32	26	20	17	18	19
m	3	4	5	6	7	8

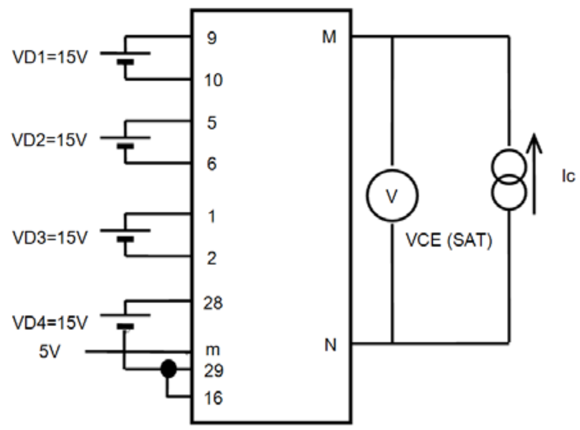


Fig.2

■ VF (Test by pulse)

	U+	V+	W+	U-	V-	W-
M	38	38	38	32	26	20
N	32	26	20	17	18	19

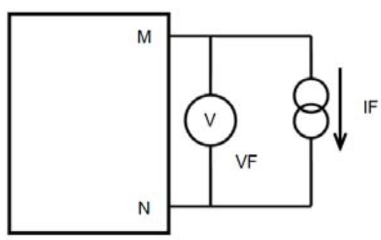


Fig.3

■RB (Test by pulse)

	U+	V+	W+
M	2	2	2
N	34	28	22
m	6	7	8

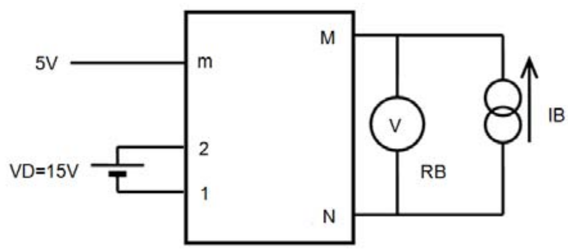


Fig.4

■ ID

	VD1	VD2	VD3	VD4
M	34	28	22	2
N	32	26	20	1

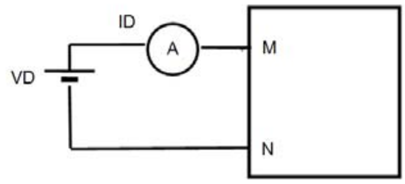
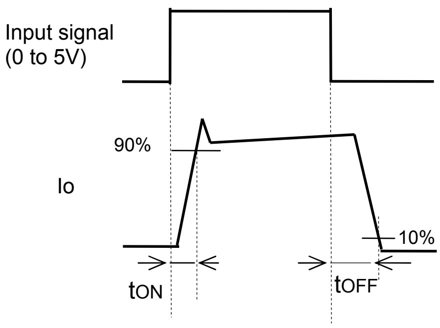


Fig.5

■ **Switching time (The circuit is a representative example of the lower side U phase.)**



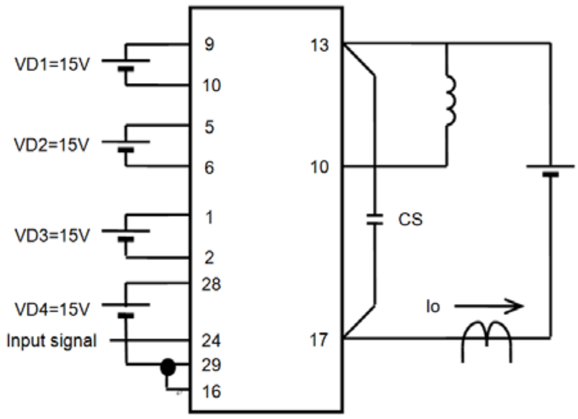


Fig.6

Input / Output Timing Chart

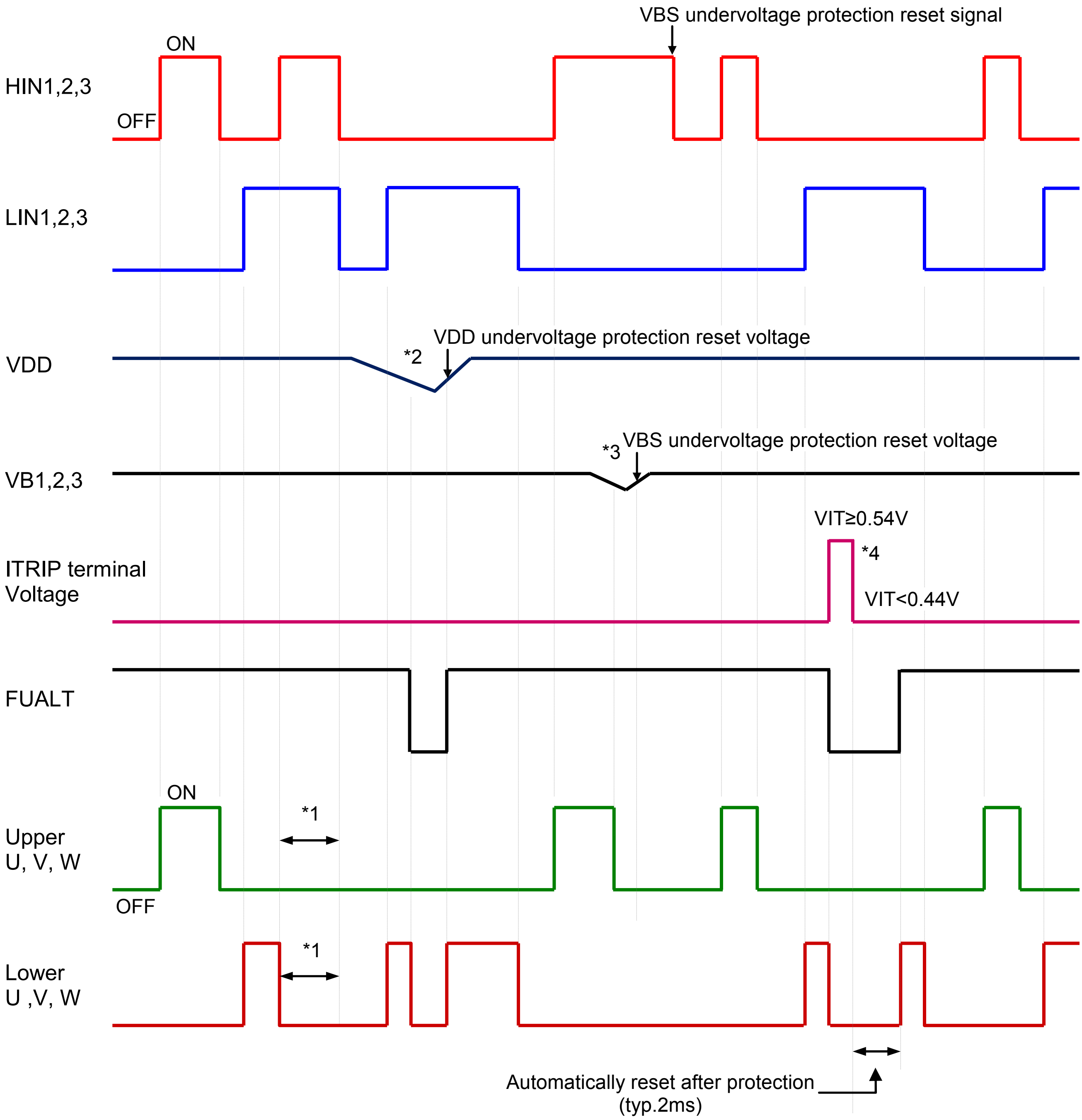


Fig. 7

Notes

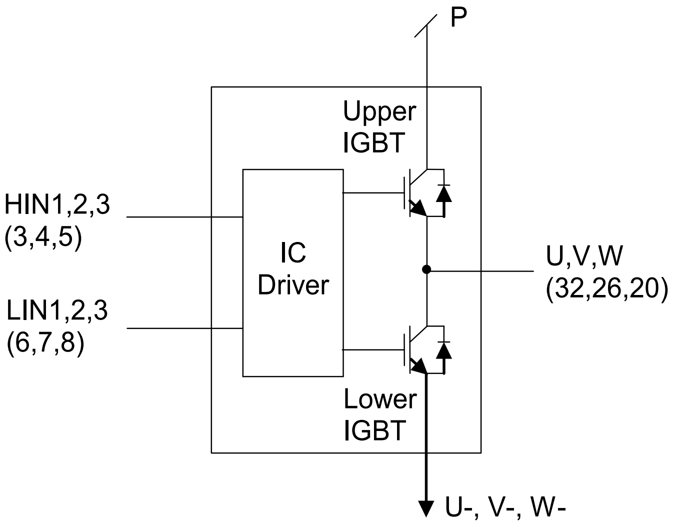
*1. Shows the prevention of shoot-thru via control logic, however, more dead time must be added to account for switching delay externally.

*2. When V_{DD} decreases all gate output signals will go low and cut off all 6 IGBT outputs. When V_{DD} rises the operation will resume immediately.

*3. When the upper side voltage at VB1, VB2 and VB3 drops only the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gate voltage rises.

*4. When VITRIP exceeds threshold all IGBT's are turned off and normal operation resumes 2ms (typ) after over current condition is removed.

Logic level table



INPUT			OUTPUT			
HIN	LIN	Itrip	Upper IGBT	Lower IGBT	U,V,W	FLTEN
H	L	L	ON	OFF	P	OFF
L	H	L	OFF	ON	U-,V-,W-	OFF
L	L	L	OFF	OFF	High Impedance	OFF
H	H	L	OFF	OFF	High Impedance	OFF
X	X	H	OFF	OFF	High Impedance	ON

Fig. 8

Sample Application Circuit

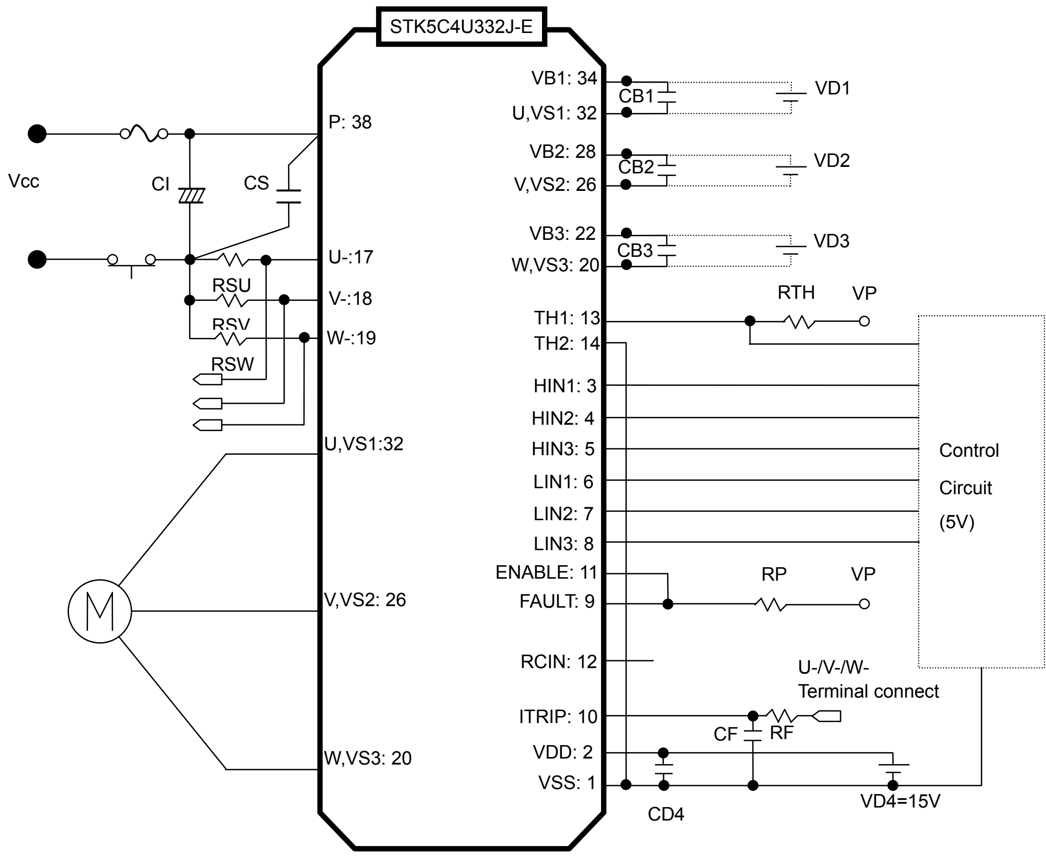


Fig.9

Recommended Operating Condition

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply voltage	V_{CC}	P to U-(V-,W-)	0	-	450	V
Pre-driver supply voltage	VD1,2,3	VB1 to U,VB2 to V,VB3 to W	12.5	15	17.5	V
	VD4	V_{DD} to V_{SS} *1	13.5	15	16.5	
ON-state input voltage	V_{IN} (ON)	HIN1,HIN2,HIN3, LIN1,LIN2,LIN3	2.5	-	-	V
OFF-state input voltage	V_{IN} (OFF)		-	-	0.8	
PWM frequency	fPWM		1	-	20	kHz
Dead time	DT	Turn-off to turn-on (external)	1.3	-	-	μs
Allowable input pulse width	PWIN	ON and OFF	1	-	-	μs
Tightening torque		'M3' type screw	0.4	-	0.6	Nm
Operating temperture	Tc	IPM case tempertre	-	-	100	°C

*1 Pre-drive power supply (VD4=15±1.5V) must have the capacity of Io=20mA (DC), 0.5A (Peak).

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Usage Precaution

1. This IPM includes bootstrap diode and resistors. Therefore, by adding a capacitor “CB”, a high side drive voltage is generated; each phase requires an individual bootstrap capacitor. The recommended value of CB is in the range of 1 to 47μF, however this value needs to be verified prior to production. If selecting the capacitance more than 47μF (±20%), connect a resistor (about 20Ω) in series between each 3-phase upper side power supply terminals (VB1,2,3) and each bootstrap capacitor.
   When not using the bootstrap circuit, each upper side pre-drive power supply requires an external independent power supply.

2. It is essential that wirning length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of “CS” is in the range of 0.1 to 10μF.

3. “FAULT” (Pin 9) is open Drain (Active Low). This terminal serves as the shut down function of the built-in pre-driver. (When the terminal voltage is above 3V, normalcy works, and it is shut down when it is equal to or less than 0.8V.) Please make pulling up outside so that “FLTEN” terminal voltages become more than 3V. When the pull up voltage (VP) is at 5V, pull up resistor (RP) recommended more than 6.8kΩ, and in case of VP=15V, RP recommended more than 20kΩ.

4. Inside the IPM, a thermistor used as the temperature monitor for internal subatrate is connected between VSS terminal and TH terminal, therefore, an external pull up resistor connected between the TH terminal and an external power supply should be used. The temperature monitor example application is as follows, please refer the Fig.10, and Fig.11 below.

5. Pull down resistor of 33kΩ is provided internally at the signal input terminals. An external resistor of 2.2k to 3.3kΩ should be added to reduce the influence of external wiring noise.

6. The over-current protection feature is not intended to protect in exceptional fault condition. An external fuse is recommended for safety.

7. “ITRIP” (Pin 10) is the input terminal of the built-in comparator. When VITRIP exceeds threshold all IGBT’s are turned off and normal operation resumes 2ms (typ) after over current condition is removed. Therefore, please do the protection movement detection of all input signals in OFF (LOW) promptly afterward.

8. When input pulse width is less than 1.0μs, an output may not react to the pulse. (Both ON signal and OFF signal)

The characteristic of thermistor

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Resistance	R_{25}	T = 25°C	99	100	101	kΩ
Resistance	R_{100}	T = 100°C	5.12	5.38	5.66	kΩ
B-Constant (25 to 50°C)	B		4165	4250	4335	K
Temperature Range			–40		+125	°C

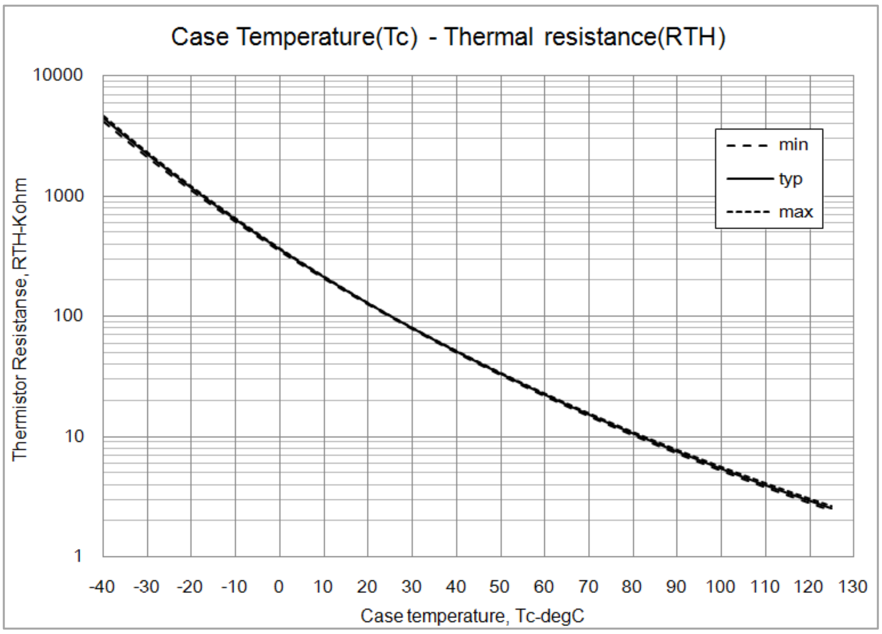


Fig.10

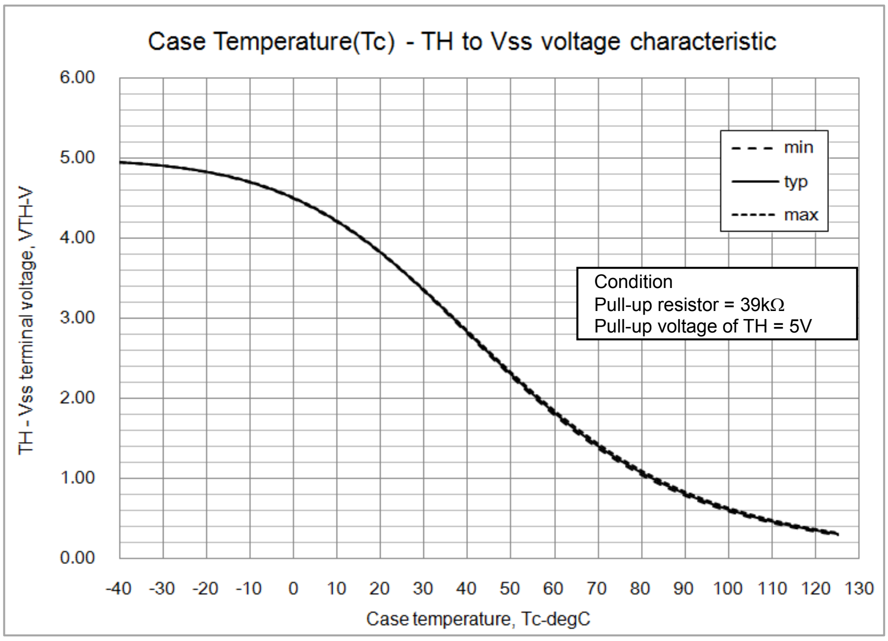


Fig.11

The characteristic of PWM switching frequency

Maximum sinusoidal phase current as function of switching frequency at Tc=100°C, VCC=300V

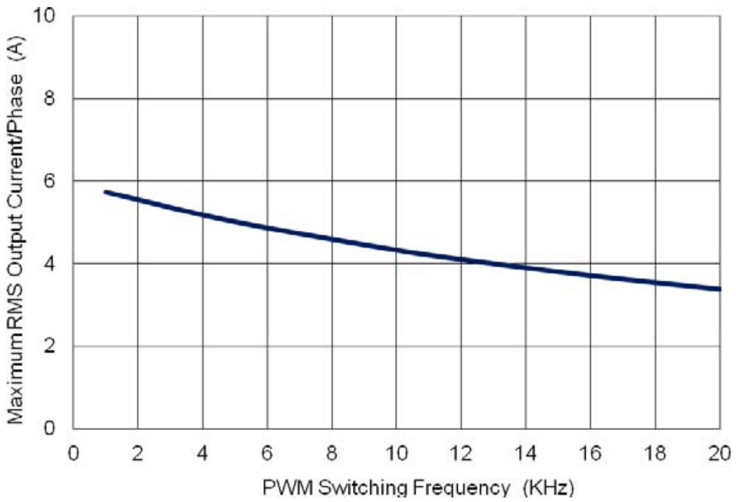


Fig.12

CB capacitor value calculation for bootstrap circuit

Calculate condition

Item	Symbol	Value	Unit
Upper side power supply.	VBS	15	V
Total gate charge of output power IGBT at 15V.	Qg	45	nC
Upper side power supply low voltage protection.	UVLO	12	V
Upper side power dissipation.	IDMAX	400	μA
ON time required for CB voltage to fall from 15V to UVLO	TONMAX	-	s

Capacitance calculation formula

Tonmax is upper arm maximum on time equal the time when the CB voltage falls from 15V to the upper limit of Low voltage protection level.
“ton-maximum" of upper side is the time that CB decreases 15V to the maximum low voltage protection of the upper side (12V).
Thus, CB is calculated by the following formula.

VBS * CB – Qg – IDMAX * TONMAX = UVLO * CB
CB = (Qg + IDMAX * TONMAX) / (VBS – UVLO)

The relationship between tonmax and CB becomes as follows. CB is recommended to be approximately 3 times the value calculated above. The recommended value of Cb is in the range of 1 to 47μF, however, the value needs to be verified prior to production.

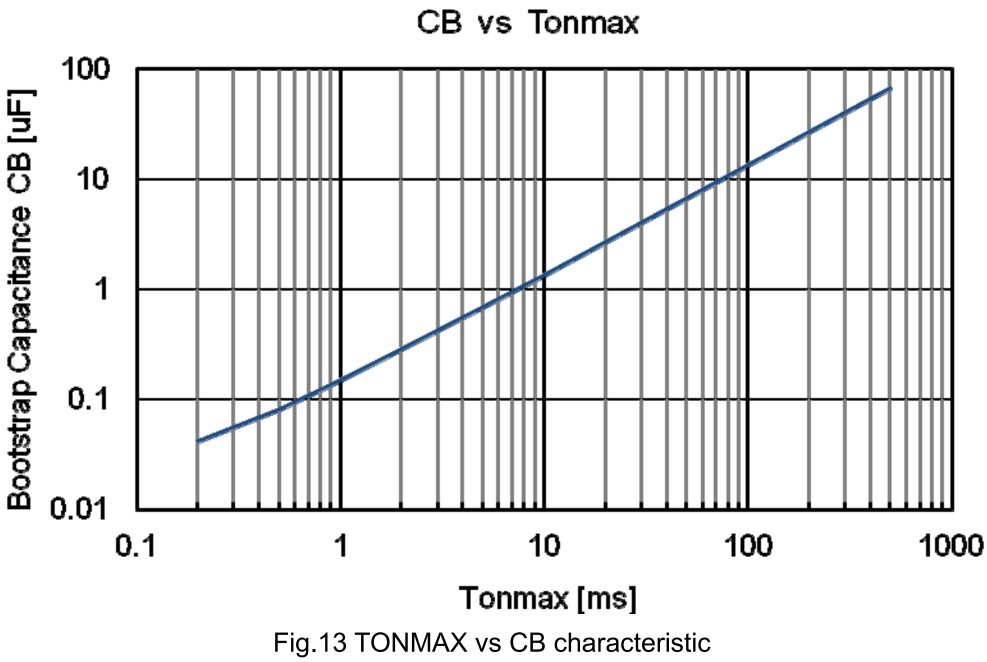
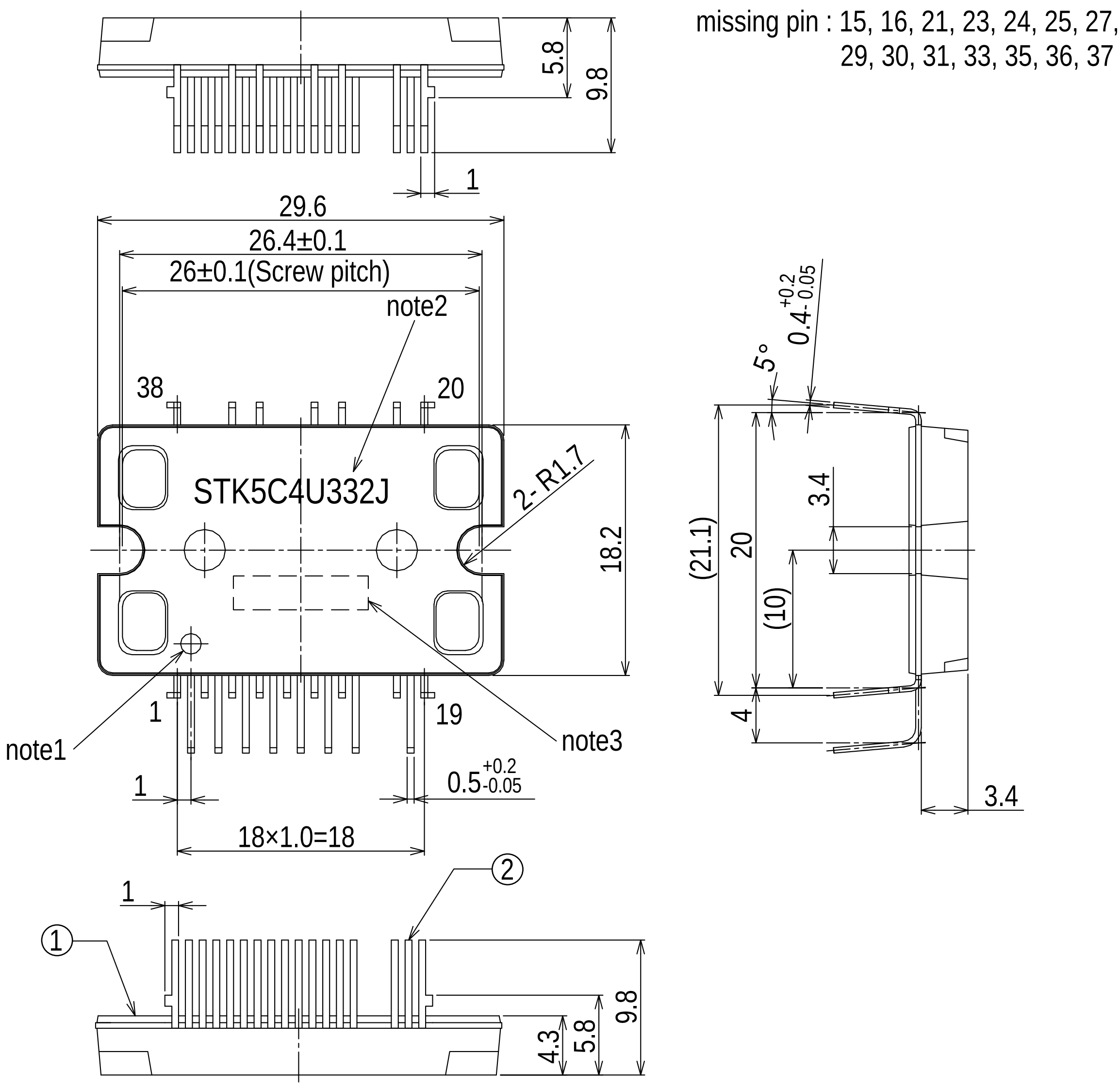


Fig.13 TONMAX vs CB characteristic

Package Dimensions

unit : mm

The tolerances of length are +/– 0.5mm unless otherwise specified.



ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK5K4U332J-E	HYBRID INTEGRATED MODULE / DIP-S (Pb-Free)	16 / Tube